

12-BIT, 21-MSPS, ULTRALOW-POWER CCD SIGNAL PROCESSOR

FEATURES

- 12-Bit, 21-MSPS, Analog-to-Digital Converter
- Low Power: 70 mW Minimum
Power-Down Mode: 4 mW
- Low Input-Referred Noise: 75-dB
SNR Typical at 0-dB Gain
- Novel Optical-Black (OB) Calibration
- Low-Aperture Delay
- Single 3-V Supply Operation
- DNL: $\leq \pm 0.5$ LSB and
INL: $\leq \pm 1.5$ LSB Typical at 0-dB Gain
- Programmable-Gain Range: 0 dB to 36 dB,
Gain Resolution of 0.05 dB/Step
- 48-Pin TQFP Package

APPLICATIONS

- Digital Still Camera
- Digital Video Camera

DESCRIPTION

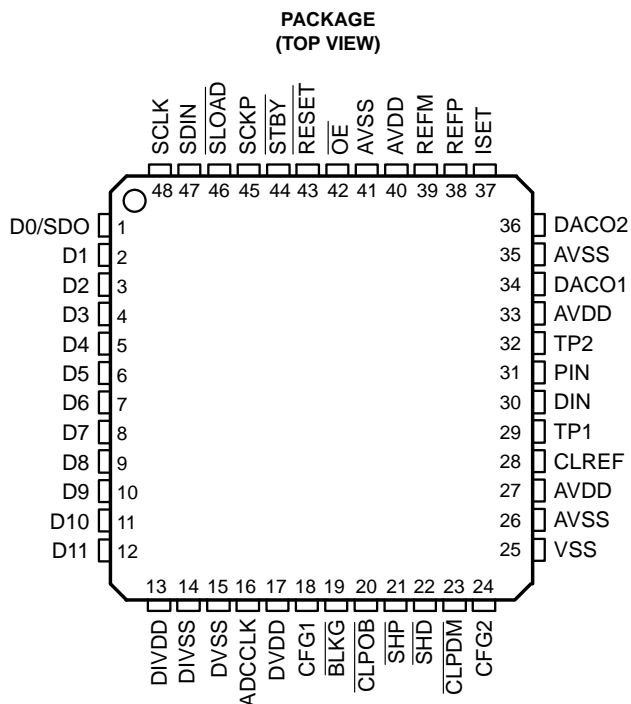
The VSP1221 is a highly-integrated mixed-signal IC used for signal conditioning and analog-to-digital conversion at the output of a CCD array. The IC has a correlated double sampler (CDS) and an analog programmable-gain amplifier (PGA) stage followed by an analog-to-digital converter (ADC) and a digital PGA stage. The CDS is used to sample the CCD signal and is followed by the analog PGA stage. The ADC is a 12-bit, 21-MSPS pipelined ADC. The digital PGA provides further amplification.

Additionally, there is an offset calibration loop for optical-black correction. The optical-black reference level is user-programmable. The chip also has two 8-bit digital-to-analog converters (DAC) for external analog settings.

The chip has a serial port for configuring internal control registers.

The VSP1221 is available in a 48-pin TQFP package and operates from a single 3-V power supply.

PIN ASSIGNMENTS



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP1221PFB	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	VSP1221	
VSP1221PFBG4	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	VSP1221	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

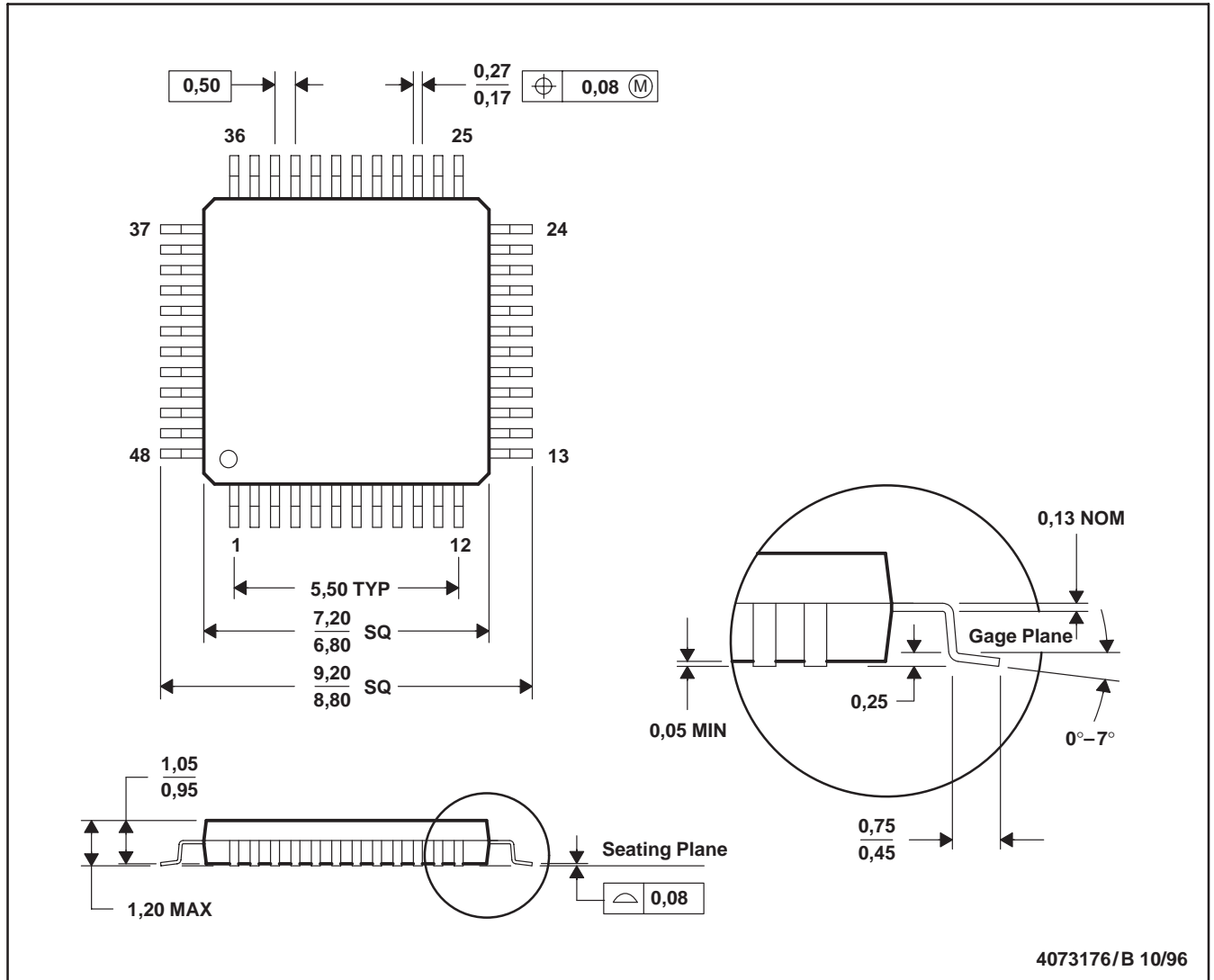
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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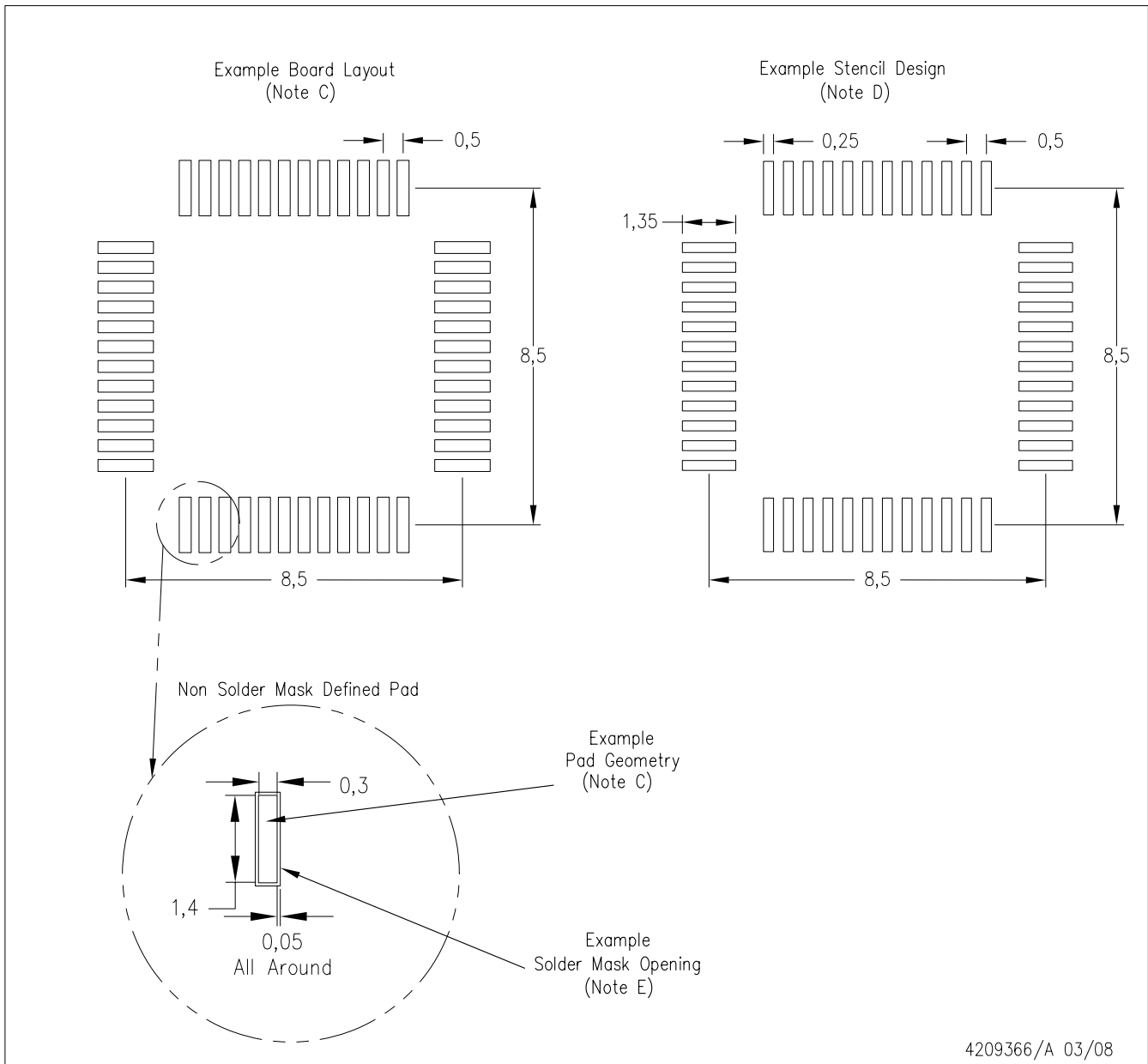
PFB (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PFB (S-PQFP-G48)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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